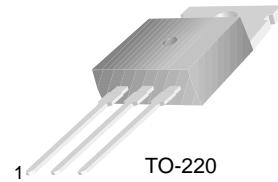


TIP115/116/117

Monolithic Construction With Built In Base-Emitter Shunt Resistors

- High DC Current Gain : $h_{FE}=1000$ @ $V_{CE}=-4V$, $I_C=-1A$ (Min.)
- Low Collector-Emitter Saturation Voltage
- Industrial Use
- Complementary to TIP110/111/112



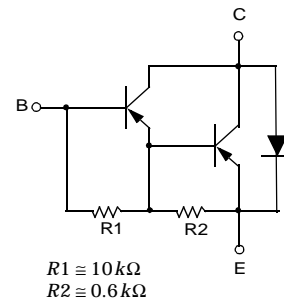
1.Base 2.Collector 3.Emmitter

PNP Epitaxial Silicon Darlington Transistor

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	: TIP115	- 60 V
		: TIP116	- 80 V
		: TIP117	- 100 V
V_{CEO}	Collector-Emitter Voltage	: TIP115	- 60 V
		: TIP116	- 80 V
		: TIP117	- 100 V
V_{EBO}	Emitter-Base Voltage	- 5	V
I_C	Collector Current (DC)	- 2	A
I_{CP}	Collector Current (Pulse)	- 4	A
I_B	Base Current (DC)	- 50	mA
P_C	Collector Dissipation ($T_a=25^\circ\text{C}$)	2	W
	Collector Dissipation ($T_C=25^\circ\text{C}$)	50	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$

Equivalent Circuit



Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	$I_C = -30\text{mA}$, $I_B = 0$: TIP115	-60	V
			: TIP116	-80	V
			: TIP117	-100	V
I_{CEO}	Collector Cut-off Current	$V_{CE} = -30V$, $I_B = 0$ $V_{CE} = -40V$, $I_B = 0$ $V_{CE} = -50V$, $I_B = 0$		-2	mA
				-2	mA
				-2	mA
I_{CBO}	Collector Cut-off Current	$V_{CB} = -60V$, $I_E = 0$ $V_{CB} = -80V$, $I_E = 0$ $V_{CB} = -100V$, $I_E = 0$		-1	mA
				-1	mA
				-1	mA
I_{EBO}	Emitter Cut-off Current	$V_{BE} = -5V$, $I_C = 0$		-2	mA
h_{FE}	DC Current Gain	$V_{CE} = -4V$, $I_C = -1A$ $V_{CE} = -4V$, $I_C = -2A$	1000		
			500		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -2A$, $I_B = -8\text{mA}$		-2.5	V
$V_{BE(on)}$	Base-Emitter ON Voltage	$V_{CE} = -4V$, $I_C = -2A$		-2.8	V
C_{ob}	Output Capacitance	$V_{CB} = -10V$, $I_E = 0$, $f = 0.1\text{MHz}$		200	pF

Typical Characteristics

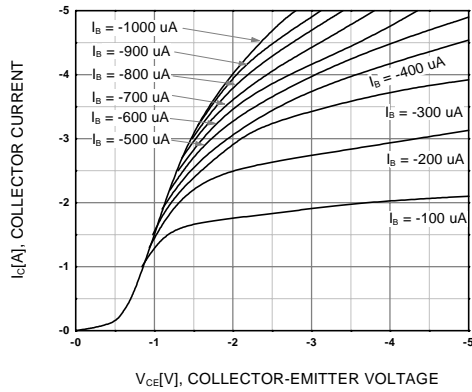


Figure 1. Static Characteristic

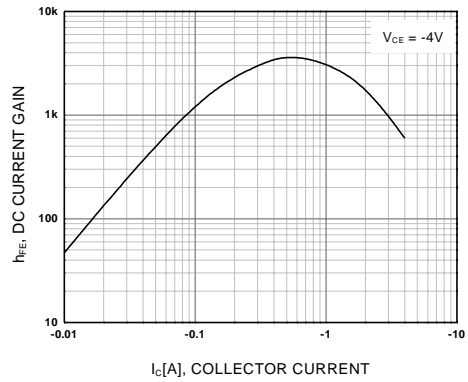


Figure 2. DC current Gain

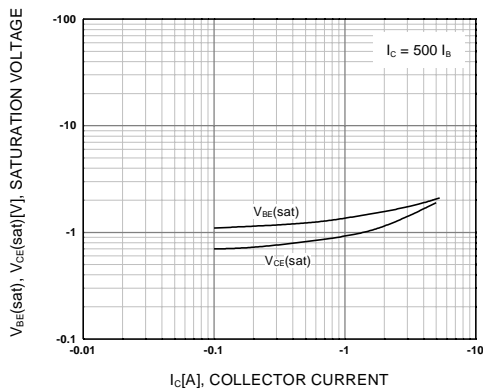


Figure 3. Collector-Emitter Saturation Voltage
Base-Emitter Saturation Voltage

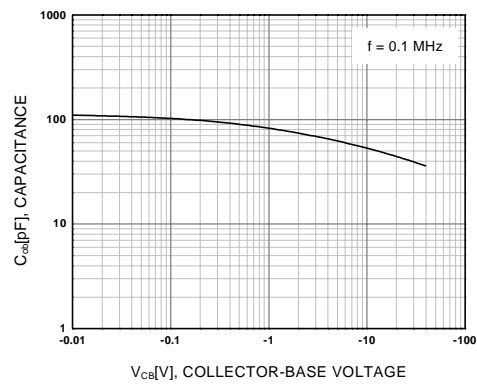


Figure 4. Collector Output Capacitance

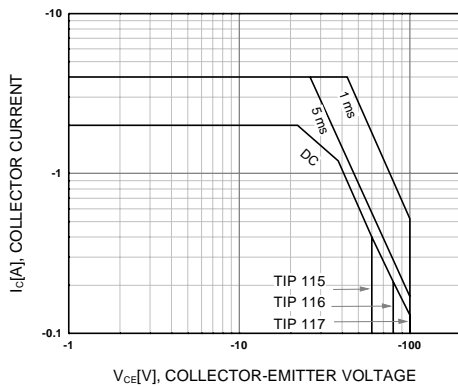


Figure 5. Safe Operating Area

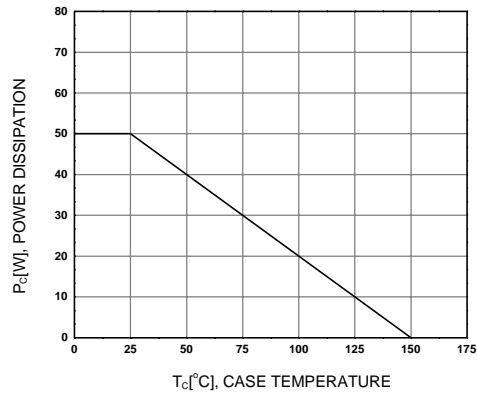
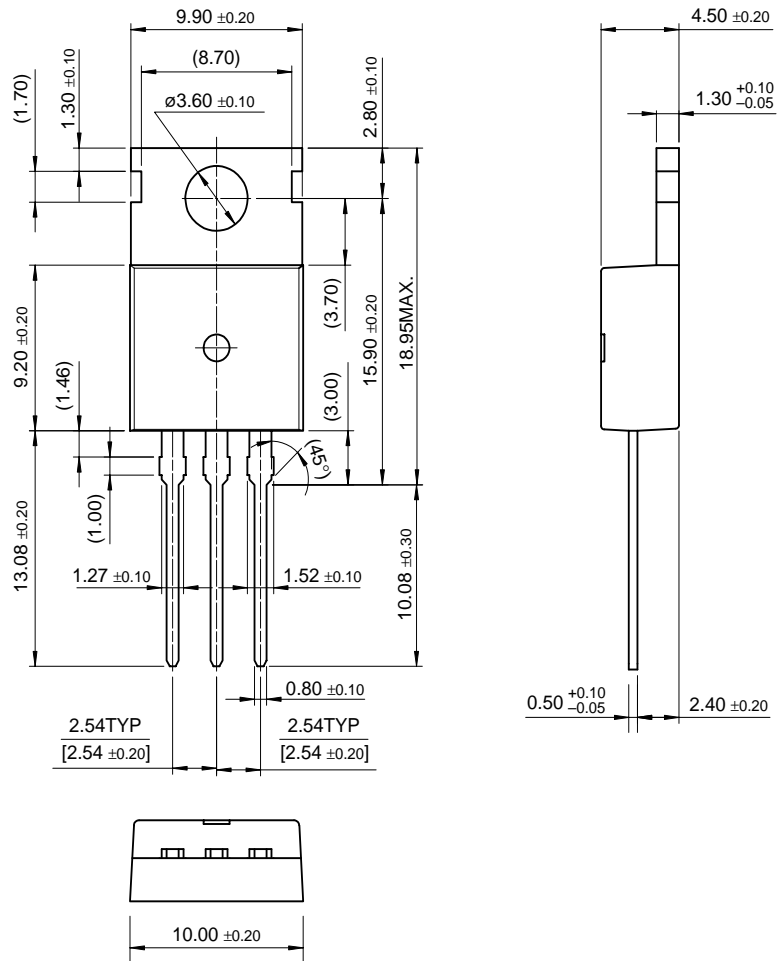


Figure 6. Power Derating

Package Dimensions

TO-220

TIP115/116/117



Dimensions in Millimeters

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E ² CMOS™	LittleFET™	QT Optoelectronics™	TinyLogic™
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