TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS017

# CD4006B Types

## CMOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output ($D_1$+4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

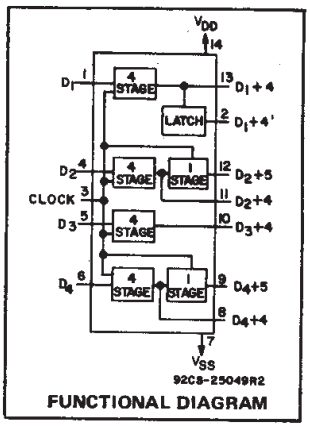
The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

*Features:*

- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD}$ = 5 V; 2 V at $V_{DD}$ = 10 V; 2.5 V at $V_{DD}$ = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

*Applications:*

- Serial shift registers
- Frequency division
- Time delay circuits




FUNCTIONAL DIAGRAM

TRUTH TABLE FOR SHIFT REGISTER STAGE

| D | CL▲ | D + 1 |
|---|---|---|
| 0 | ↓ | 0 |
| 1 | ↓ | 1 |
| X | ↓ | NC |

TRUTH TABLE FOR OUTPUT FROM TERM.2

| $D_1$+4 | CL▲ | $D_1$+4' |
|---|---|---|
| 0 | ↑ | 0 |
| 1 | ↑ | 1 |
| X | ↓ | NC |

1 = HIGH; 0 = LOW; NC = NO CHANGE; X = DON'T CARE; ▲ = LEVEL CHANGE

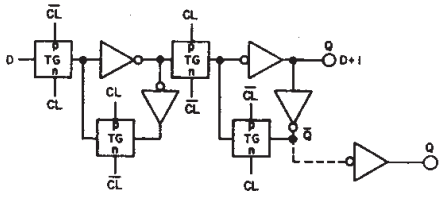
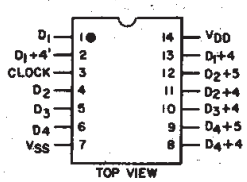
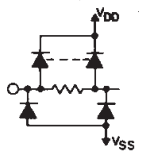



*Fig. 1 — Logic diagram and truth table (one register stage).*

**TERMINAL ASSIGNMENT**




ALL INPUTS (TERMINALS 1,3,4,5,6) PROTECTED BY CMOS PROTECTION NETWORK

92CS-28974

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS Min. | LIMITS Max. | UNITS |
|---|---|---|---|---|
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) | – | 3 | 18 | V |
| Clock Pulse Width, $t_W$ | 5 | 180 | – | ns |
| | 10 | 80 | – | |
| | 15 | 50 | – | |
| Data Setup Time, $t_S$ | 5 | 100 | – | ns |
| | 10 | 50 | – | |
| | 15 | 40 | – | |
| Data Hold Time, $t_H$ | 5 | 60 | – | ns |
| | 10 | 40 | – | |
| | 15 | 30 | – | |
| Clock Rise or Fall Time: $t_r$, $t_f$ | 5,10, 15 | – | 15 | μS |
| Clock Input Frequency, $f_{CL}$ | 5 | – | 2.5 | MHz |
| | 10 | – | 5 | |
| | 15 | – | 7 | |

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

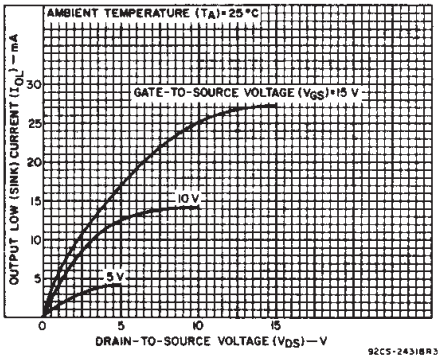



*Fig. 2 – Typical output low (sink) current characteristics.*

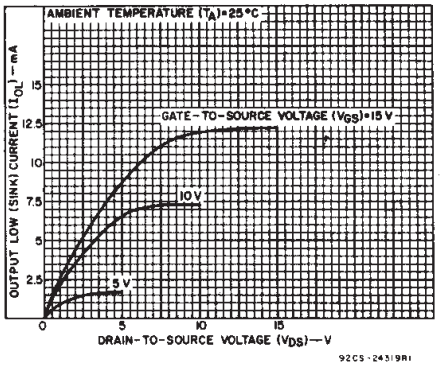



*Fig. 3 – Minimum output low (sink) current characteristics.*

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | 0,10 | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | 0,15 | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | 0,20 | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3 4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | – | |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | – | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | – | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | – | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1, 9 | – | 10 | 3 | | | | — | — | 3 | |
| | 1.5,13.5 | – | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5, 4.5 | – | 5 | 3.5 | | | | 3.5 | — | — | |
| | 1, 9 | – | 10 | 7 | | | | 7 | — | — | |
| | 1.5,13.5 | - | 15 | 11 | | | | 11 | — | — | |
| Input Current $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $\pm 10^{-5}$ | ±0.1 | μA |

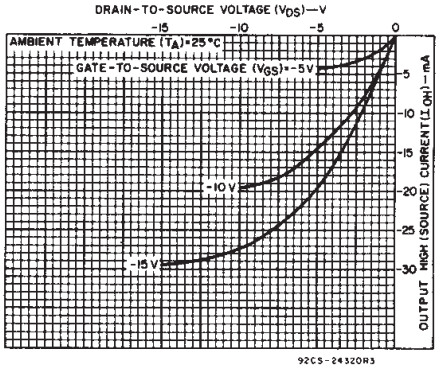



*Fig. 4 – Typical output high (source) current characteristics.*

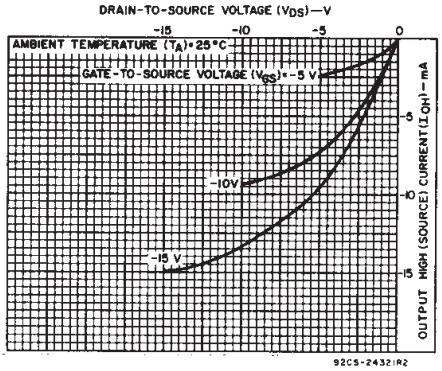



*Fig. 5 – Minimum output high (source) current characteristics.*

**DYNAMIC ELECTRICAL CHARACTERISTICS** *at $T_A$ = 25°C; Input $t_r$,$t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ*

| CHARACTERISTIC | TEST CONDITIONS $V_{DD}$ (V) | LIMITS MIN. | LIMITS TYP. | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|
| Propagation Delay Time, $t_{PHL}$, $t_{PLH}$ | 5 | — | 200 | 400 | ns |
| | 10 | — | 100 | 200 | |
| | 15 | — | 80 | 160 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Data Setup Time, $t_s$ | 5 | — | 50 | 100 | ns |
| | 10 | — | 25 | 50 | |
| | 15 | — | 20 | 40 | |
| Minimum Clock Pulse Width, $t_w$ | 5 | — | 100 | 200 | ns |
| | 10 | — | 45 | 90 | |
| | 15 | — | 30 | 60 | |
| Maximum Clock Input Frequency, $f_{CL}$ | 5 | 2.5 | 5 | — | MHz |
| | 10 | 5 | 10 | — | |
| | 15 | 7 | 14 | — | |
| Maximum Clock Input Rise or Fall Time, $t_rCL$, $t_fCL$* | 5 | — | — | 15 | μs |
| | 10 | — | — | 15 | |
| | 15 | — | — | 15 | |
| Input Capacitance, $C_{IN}$ | Any Input | — | 5 | 7.5 | pF |

*If more than one unit is cascaded $t_rCL$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

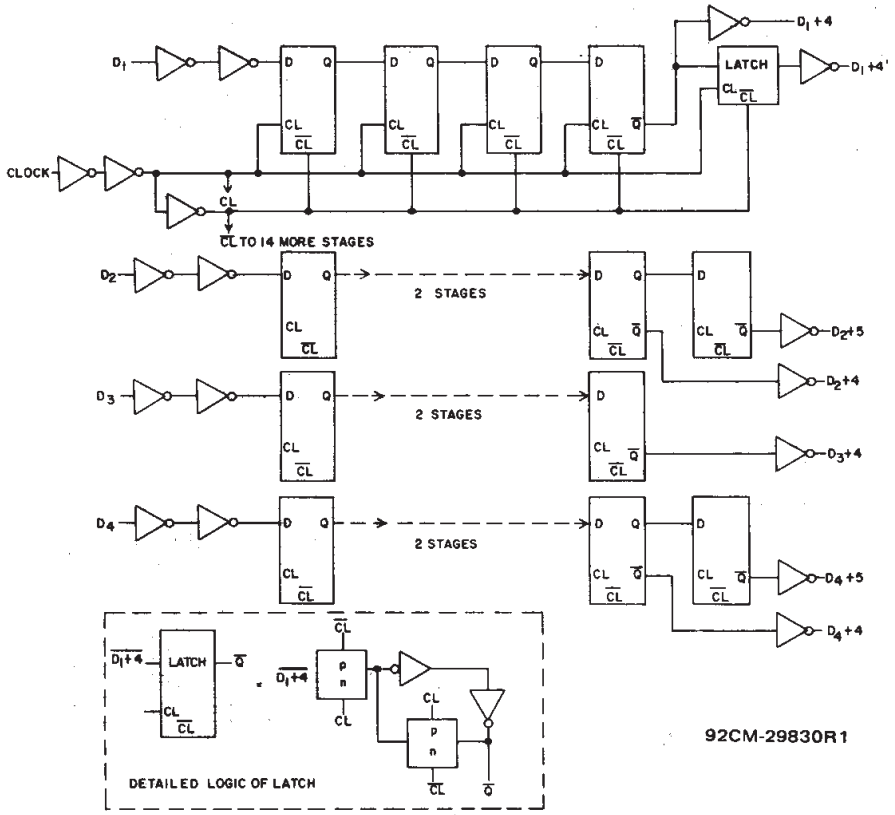



*Fig. 6 – Logic diagram with detail of latch.*

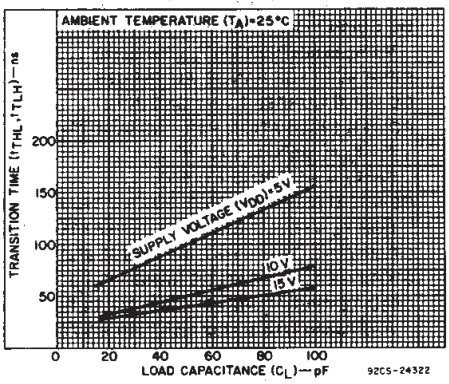



*Fig. 7 – Typical transition time as a function of load capacitance.*

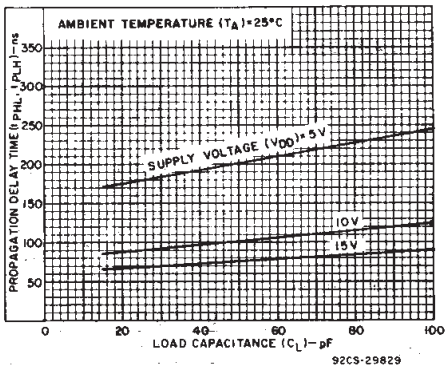



*Fig. 8 – Typical propagation delay time as a function of load capacitance.*

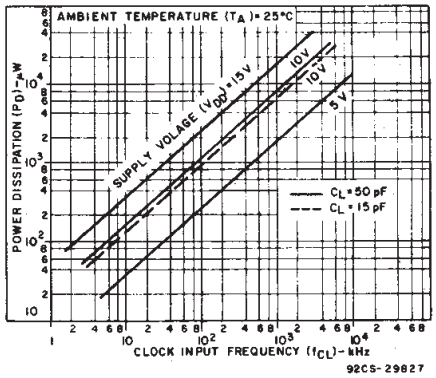



*Fig. 9 – Typical dyanamic power dissipation as a function of clock frequency.*

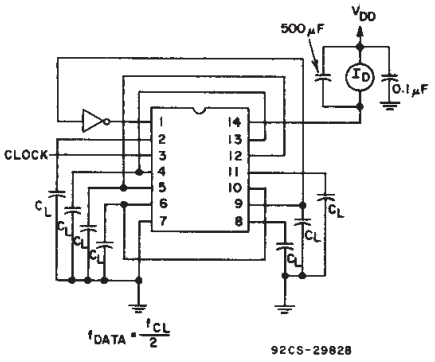



Fig. 10 – Dynamic power dissipation test circuit.

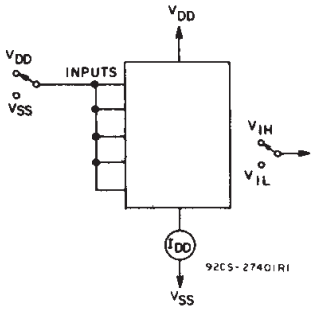



Fig. 11 – Quiescent device current test circuit.

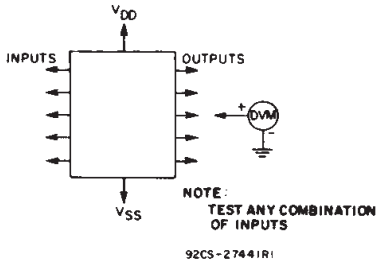



Fig. 12 – Input voltage test circuit.

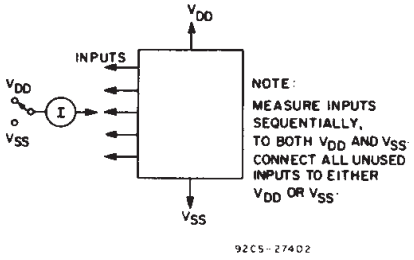
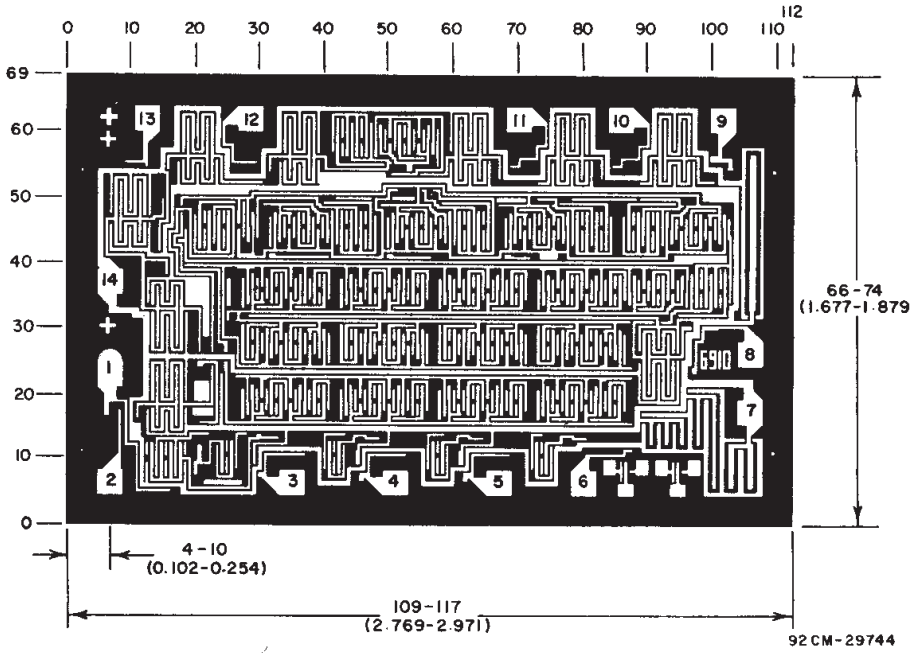



Fig. 13 – Input current test circuit.




*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

*Dimensions and pad layout for CD4006BH.*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD4006BE | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| CD4006BF3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

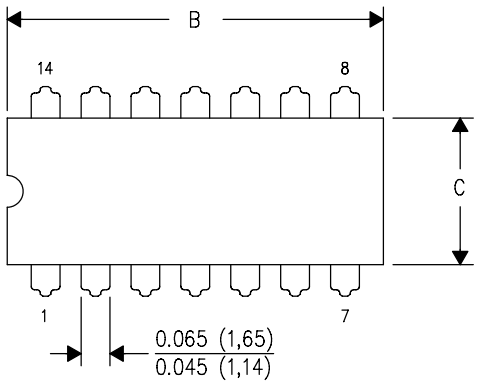
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

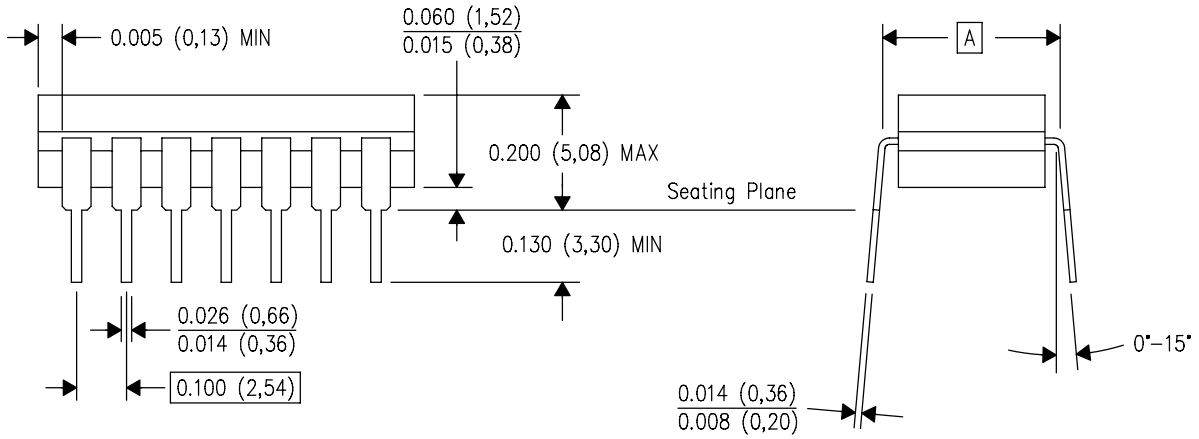
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



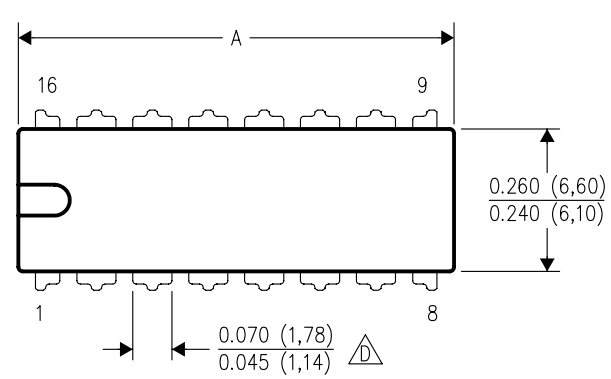

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

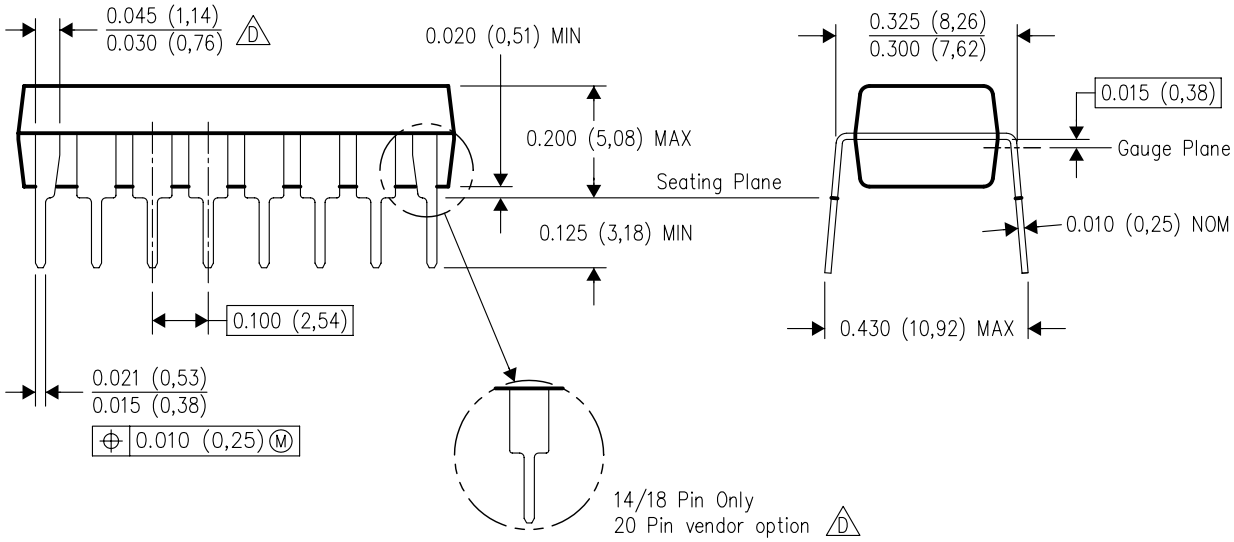
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| Low Power Wireless | www.ti.com/lpw | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
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